WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate having a surface;

a gate insulating layer formed over the surface of the semiconductor substrate; and

a gate electrode formed over the gate insulating layer;

wherein the gate electrode includes a lower poly-SiGe layer having a columnar crystalline structure, and an upper poly-Si layer having a random crystalline structure.

2. The device of claim 1, wherein a grain size of the upper poly-Si layer is larger than a grain size of the lower poly-SiGe layer.

3. The device of claim 1, wherein a grain size of the upper poly-Si layer in a direction horizontal to the surface of the semiconductor substrate is at least as great as a grain size of the upper poly-Si layer in a direction vertical to the surface of the semiconductor substrate.

4. The device of claim 1, further comprising a seed layer interposed between the lower poly-SiGe layer and the gate insulating layer.

5. The device of claim 1, further comprising at least one intermediate layer interposed between the upper poly-Si layer and the lower poly-SiGe layer.

6. The device of claim 5, wherein the at least one intermediate layer includes a Si layer.

7. The device of claim 5, wherein the at least one intermediate layer includes a SiGe layer.

8. The device of claim 5 wherein the at least one intermediate layer includes a Si layer and a SiGe layer.

9. A semiconductor device comprising:

a semiconductor substrate having a surface;

a gate insulating layer formed over the surface of the semiconductor substrate; and

a gate electrode formed over the gate insulating layer;

wherein the gate electrode includes a lower poly-SiGe layer having a columnar crystalline structure, an intermediate layer having an random crystalline structure, and an upper poly-Si layer having a columnar crystalline structure.

10. The device of claim 9, wherein the intermediate layer is a poly-Si layer.

11. The device of claim 9, wherein the intermediate layer is a poly-SiGe layer.

12. The device of claim 9, wherein a grain size of the intermediate layer is larger than a grain size of the lower poly-SiGe layer.

13. A method of manufacturing a semiconductor device, comprising:

depositing a gate insulating layer over a surface of a semiconductor substrate;

depositing a lower poly-SiGe layer having a columnar crystalline structure over the gate insulating layer;

depositing an amorphous Si layer over the lower poly-SiGe layer; and

crystallizing the amorphous Si layer to obtain an upper poly-Si layer having a random crystalline structure.

14. The method of claim 13, wherein the lower poly-SiGe layer is deposited by CVD at a temperature range of 400°C to 600°C.

15. The method of claim 13, wherein the lower poly-SiGe layer is deposited by chemical vapor deposition of SiH_4 and GeH_4 at a temperature range of 400°C to 600°C.

16. The method of claim 13, wherein the lower poly-SiGe layer is deposited by chemical vapor deposition of Si_2H_6 and GeH_4 at a temperature range of 400°C to 600°C.

17. The method of claim 13, wherein the amorphous Si layer is deposited by CVD at a temperature range of 350°C to 580°C.

18. The method of claim 13, further comprising, prior to crystallizing the amorphous Si layer, patterning the lower poly-SiGe layer and the amorphous Si layer to define a gate electrode.

19. The method of claim 13, further comprising, after crystallizing the amorphous Si layer, patterning the lower poly-SiGe layer and the upper poly-Si layer to define a gate electrode.

20. The method of claim 13, further comprising depositing a seed layer on the surface of the semiconductor layer prior to depositing the lower poly-SiGe layer.

21. The method of claim 13, wherein the amorphous Si layer is crystallized by an anneal process.

22. A method of manufacturing a semiconductor device, comprising:

depositing a gate insulating layer over a surface of a semiconductor substrate;

depositing a lower poly-SiGe layer having a columnar crystalline structure over the gate insulating layer;

depositing at least one intermediate layer having an amorphous structure over the lower poly-SiGe layer;

depositing an amorphous Si layer over the at least one intermediate layer; and

crystallizing the amorphous Si layer to obtain an upper poly-Si layer having a random crystalline structure.

23. The method of claim 22, wherein the at least one intermediate layer is another amorphous Si layer.

24. The method of claim 22, wherein the at least one intermediate layer is an amorphous SiGe layer.

25. The method of claim 24, wherein the amorphous SiGe layer is deposited by CVD at a temperature range of 350°C to 500°C.

26. The method of claim 24, wherein the amorphous SiGe layer is deposited by CVD of (SiH_4 or Si_2H_6) and GeH_4 at a temperature range of 350°C to 500°C.

27. The method of claim 22, wherein the at least one intermediate layer includes a first intermediate layer and a second intermediate layer, wherein the first intermediate layer is another amorphous Si layer and the second intermediate layer is an amorphous SiGe layer.

28. The method of claim 22, wherein the amorphous Si layer is deposited by CVD at a temperature range of 350°C to 580°C.

29. The method of claim 22, wherein the amorphous Si layer is deposited by CVD of SiH_4 or Si_2H_6 at a temperature range of 350°C to 580°C.

30. A method of manufacturing a semiconductor device, comprising:

depositing a gate insulating layer over a surface of a semiconductor substrate;

depositing a lower poly-SiGe layer having a columnar crystalline structure over the gate insulating layer;

depositing an amorphous intermediate layer over the lower poly-SiGe layer;

depositing an upper poly-Si layer over the amorphous intermediate layer; and

crystallizing the amorphous intermediate layer to obtain a crystallized intermediate layer having a random crystalline structure between the lower poly-SiGe layer and the upper poly-Si layer.